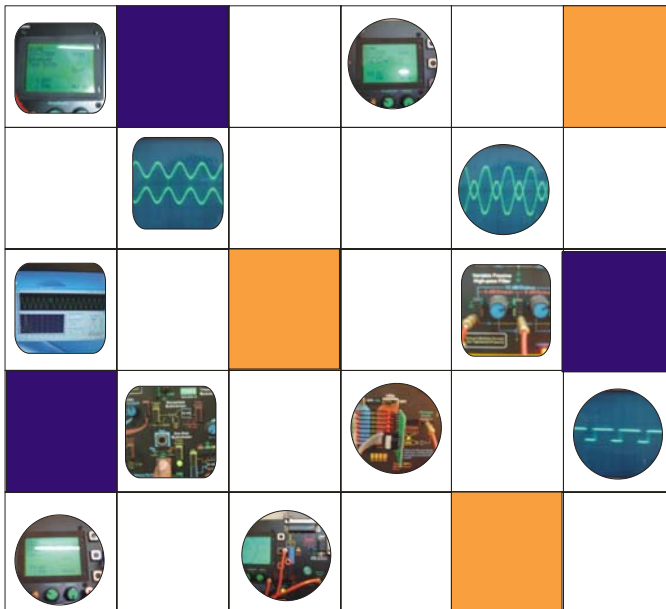


RIMSResearch Instrumentation
& Measurement Systems**DEV-2765**

Digital Electronics Trainer

EXPERIMENTS

PART NO. 2765-00-321



**COMPREHENSIVE AND ILLUSTRATED
EASY EXPERIMENTS STARTUP**

LAB MANUAL

THANK YOU FOR CHOOSING RIMS EDUCATION PRODUCTS AND SERVICES

Once you have made it through this guide, you will have a firm grip on your lab experiments and operations of the RIMS product you are using. How to get your training equipment operational, basic maintenance and setting up desired experiments will just be a breeze. Everything you need for a quick and easy start is presented here—useful hints and tips makes it simple to conduct your lab and hands-on training sessions. We are happy that you have joined our vast community of over 30 thousand valued users, which grow as we bring you the latest technology at most competitive prices. We value your business and hope that you will enjoy being an important member of the RIMS Education Community.

Customer Support Team



EU, USA and Canada

Weston Villa, 37 Wolsey Road, Esher, Surrey
United Kingdom KT10 8NT

www.rims-tech.co.uk

Middle East & Asia Pacific

632-B Chakala Scheme-III Rawalpindi
Pakistan 46000

www.rimsedu.com

© RIMS 1999-2007. All Rights Reserved. No part of this manual is to be copied, modified or sold in any form without prior permission of RIMS EDUCATION for any further queries please visit our website at <http://www.rims-tech.co.uk>

WARRANTY

The media on which you receive RIMS Technologies software/hardware are warranted for defects in materials and workmanship, for a period of 90 days from date of shipment, as evidenced by receipts or other documentation. RIMS Technologies will, at its option, repair or replace software/hardware media that do not execute programming instructions if RIMS Technologies receives notice of such defects during the warranty period. RIMS Technologies does not warrant that the operation of the software/hardware shall be uninterrupted or error free.

A Return Material Authorization (RMA) number must be obtained from the factory and clearly marked on the outside of the package before any equipment will be accepted for warranty work. RIMS Technologies will pay the shipping costs of returning to the owner parts which are covered by warranty.

RIMS Technologies believes that the information in this document is accurate. The document has been carefully reviewed for technical accuracy. In the event that technical or typographical errors exist, RIMS Technologies reserves the right to make changes to subsequent editions of this document without prior notice to holders of this edition. The reader should consult RIMS Technologies if errors are suspected.

In no event shall RIMS Technologies be liable for any damages arising out of or related to this document or the information contained in it. EXCEPT AS SPECIFIED HEREIN, RIMS TECHNOLOGIES MAKES NO WARRANTIES, EXPRESS OR IMPLIED, AND SPECIFICALLY DISCLAIMS ANY WARRANTY OF MERCHANTABILITY OR FITNESS FOR A PARTICULAR PURPOSE. RIMS TECHNOLOGIES WILL NOT BE LIABLE FOR DAMAGES RESULTING FROM LOSS OF DATA, PROFITS, USE OF PRODUCTS, OR INCIDENTAL OR CONSEQUENTIAL DAMAGES, EVEN IF ADVISED OF THE POSSIBILITY THEREOF. This limitation of the liability of RIMS Technologies will apply regardless of the form of action, whether in contract or tort, including negligence. Any action against RIMS Technologies must be brought within one year after the cause of action accrues. RIMS Technologies shall not be liable for any delay in performance due to causes beyond its reasonable control. The warranty provided herein does not cover damages, defects, malfunctions, or service failures caused by owner's failure to follow the RIMS Technologies installation, operation, or maintenance instructions; owner's modification of the product; owner's abuse, misuse, or negligent acts; and power failure or surges, act of God, fire, flood, accident, actions of third parties, or other events outside reasonable control.

COPYRIGHT

Under the copyright laws, this publication may not be reproduced or transmitted in any form, electronic or mechanical, including photocopying, recording, storing in an information retrieval system, or translating, in whole or in part, without the prior written consent of RIMS Technologies.

TRADEMARKS

RIMS™, ThinPoint™, Power to Sense and Control™, INSPTEP™, LiveLabs™, RIMS Technologies™, BOX™, RIMS-Scope™, StateView™, rims-tech.co.uk™, RIMS-DAQ™, RIMS Students Zone™, and RIMS-Passport™ are trademarks of RIMS Technologies.

Product and company names mentioned herein are trademarks or trade names of rims technologies.

PATENTS

For patents covering RIMS Technologies products, refer to the RIMS Website www.rims-tech.co.uk.

WARNING REGARDING USE OF RIMS TECHNOLOGIES PRODUCTS

(1) RIMS Technologies products are not designed with components and testing for a level of reliability suitable for use in or in connection with surgical implants or as critical components in any life support systems whose failure to perform can reasonably be expected to cause significant injury to a human and also for industrial or specify critical application.

(2) In any application, including the above, reliability of operation of the software/hardware products can be impaired by adverse factors, including but not limited to fluctuations in electrical power supply, computer hardware malfunctions, computer operating system software/hardware fitness, fitness of compilers and development software/hardware used to develop an application, installation errors, software and hardware compatibility problems, malfunctions or failures of electronic monitoring or control devices, transient failures of electronic systems (hardware and/or software), unanticipated uses or misuses, or errors on the part of the user or applications designer (adverse factors such as these are hereafter collectively termed "system failures"). Any application where a system failure would create a risk of harm to property or persons (including the risk of bodily injury and death) should not be reliant solely upon one form of electronic system due to the risk of system failure. To avoid damage, injury, or death, the user or application designer must take reasonably prudent steps to protect against system failures, including but not limited to back-up or shut down mechanisms. Because each end-user system is customized and differs from rims technologies' testing platforms and because a user or application designer may use rims technologies products in combination with other products in a manner not evaluated or contemplated by rims technologies, the user or application designer is ultimately responsible for verifying and validating the suitability of rims technologies products whenever rims technologies products are incorporated in a system or application, including, without limitation, the appropriate design, process and safety level of such system or application.

(3) All efforts have been done to ensure the correctness of the information or media provided explicitly or implicitly for each training system. However RIMS technologies do not take any responsibility for the losses or otherwise any issues arising from the mistake in the media provided. RIMS would strive to ensure that the mistakes are corrected and communicated to all its customers.

Welcome to RIMS Digital Electronics Trainer

- Fundamental Logic Gates- AND, OR, NOT
- Fundamental Logic Gates- NAND, NOR, XOR
- De Morgan's Law (1)
- De Morgan's Law (11)
- Application of Boolean Algebra
- Diode Resister Logic – AND
- Exclusive OR Using Basic Logic Gates
- Exclusive NOR Using basic Logic Gate
- Demultiplexer – Using The 74138 IC
- Synchronous Up – Counter
- Synchronous Down – Counter
- The Schmitt Trigger
- Oscillator – Using CMOS

Product Title: EXPERIMANTS WORK BOOK

Document Code: DEV2765-00-321

Revision 2.0.0 dated January 2007

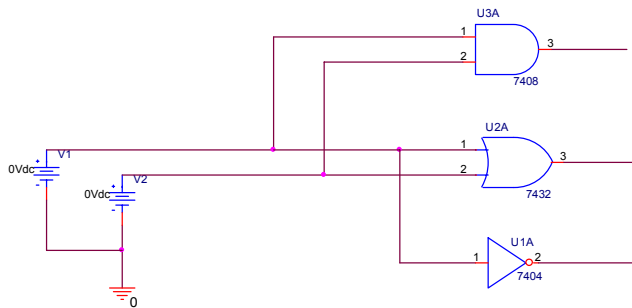
© RIMS 1999-2007. All Rights Reserved. No part of this manual is to be copied, modified or sold in any form without prior permission of RIMS EDUCATION for any further queries please visit our website at <http://www.rims-tech.co.uk>

STEP 1**FUNDAMENTAL LOGIC GATES- AND, OR, NOT****Purpose:**

To show the input and output relationship of 2-input AND, OR, and 1-input NOT gates by constructing their truth tables.

Required Components and Equipments:

1. 7404×1, 7408×1, 7432×1
2. RIMS Trainer DEV-2765E

Diagram of Circuit:**Fig. 1-1****Procedure:**

Step 1: Construct the circuit of Fig1-1 on the breadboard. Remember each IC's pin 14 is connected to "+5V" DC Power Supply and pin 7 to "GND" position.

Step 2: Connect the inputs of the gates to digital switches "0" and "1". Next, connect 12 Bit LED Display's "0", "1", and "2" position to the outputs of different gates of Fig2-1, respectively.

Step 3: Change Data Switches "0" and "1" between "0" and "1" position, and observe the situation of 12 Bit LED Display "0", "1", and "2". The LED light that indicates the output in the logic 1 condition. When LED is dark it indicates that the output is in the logic 0 conditions.

Step 4: The inputs and outputs in the form of a truth table as shown in table 1-1

A	B	Y1	Y2	Y3
0	0	0	0	1
0	1	0	1	1
1	0	0	1	0
1	1	1	1	0

Table 1-1

STEP 2	FUNDAMENTAL LOGIC GATES- NAND, OR, XOR
---------------	--

Purpose:

To demonstrate the input and outputs relationship of 2-input NAND, NOR gates by constructing their truth table.

Required Components and Equipments:

1. 7404×1, 7408×1, 7432×1 functions of IC's.
2. RIMS Trainer DEV-2765

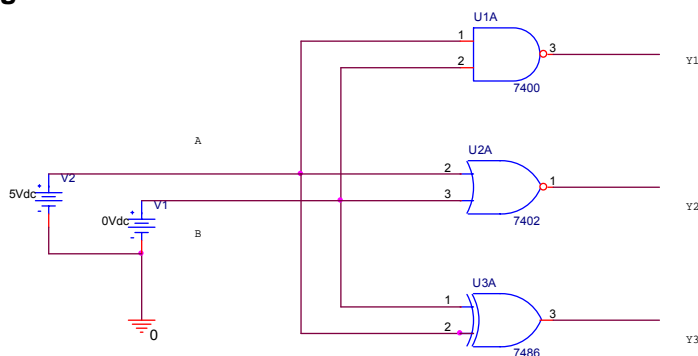
Diagram of Circuit:

Fig. 2-1

Procedure:

Step 1: Construct the component of fig 2-1 onto the breadboard of your trainer, and properly link the connections.

Remember to connect IC's pin 14 to "+5v" socket and pin 7 to "GND" socket.

Step 2: Connect the data Switches "0" and "1" to point A and B of fig, 2-1, respectively. Then , connect 12 Bit LED Display's "0", "1", and "2" position to the output of point Y1, Y2, and Y3 of Fig2-1.

Step 3: Change Data Switches "0" and "1" between "0" and "1" position , and observe the situation of 12 Bit LED Display "0" , "1" ,and "2". The LED light that indicates the output in the logic 1 condition When LED is dark it indicates that the output is in the logic 0 conditions.

Step 4: Record the result that you have observed into the truth table of Fig2-2.

Result: If you have wired everything correctly, the output of the three gates should be as follow:

A	B	Y1	Y2	Y3
0	0	1	1	0
0	1	1	0	1
1	0	1	0	1
1	1	0	0	0

Table 2-2

If not, recheck your circuit on breadboard and power supply, and then repeat this experiment, and find out the problem.

STEP 3**DE MORGAN'S LAW (I)****Purpose:**

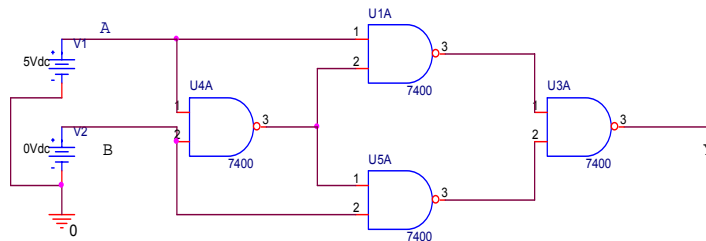
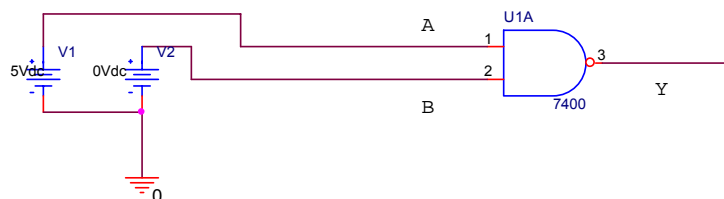
To verify the De Morgan's Law $(AB)' = \bar{A} + \bar{B}$.

Theory

One of De Morgan's Law is $(AB)' = \bar{A} + \bar{B}$. This means that the NAND gate function is equivalent to the OR gate function with complement input of A and B from this experiment you can understand how to exchange gates for other gates.

Required Components and Equipments:

1. 7404×1, 7408×1, 7432×1
2. RIMS Trainer DEV-2765

Diagram of Circuit:**(A)****(B)****Procedure:**

Step 1: Construct the circuit shown in Fig. 3-1 (a) and Fig.3-1(b) on the breadboard like as Fig. 3-2.

Step 2: Connect input point A and B to any of the Data switches and point Y to the logic probe

Step 3: Switch on the system and using all possible binary inputs tabulate the result as shown in table 3-1.

A	B	$Y=\overline{AB}$	$Y=\overline{A+B}$
0	0	1	1
0	1	1	1
1	0	1	1
1	1	0	0

Table 3-1**Application:**

Construct a circuit of \overline{AB} and verify through experiment that the circuit of \overline{AB} is logic identical to the circuit of $\overline{A+B}$.

STEP 4**DE MORGAN'S LAW (II)****Purpose:**

To verify the De Morgan's Law is that $(A+B)' = \overline{A} \overline{B}$.

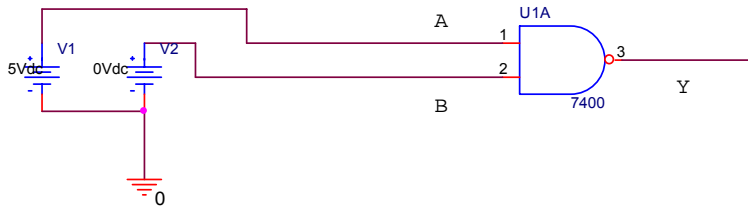
Theory:

One of De Morgan's Law is $(A+B)' = \overline{A} \overline{B}$. This means that the NOR gate function is equal to the AND gate function with complement input of A and B.

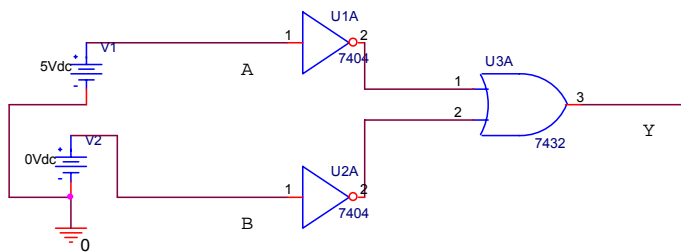
Required Components and Equipments:

1. 7402×1, 7404×1, 7432×1
2. RIMS Training System

Diagram of Circuit:



(A)



(B)

Procedure:

Step 1: Construct the circuit show in Fig. 4-1 (a) and Fig.4-1(b) on the breadboard.

Step 2: Connect input points A and B to any of the Data switches and point Y to the logic probe.

Step 3: Switch on the system and using all possible binary inputs tabulate the result as shown in table 4-1.

A	B	$Y=A+B$	$\bar{Y}=\bar{A} \bar{B}$
0	0	1	1
0	1	0	0
1	0	0	0
1	1	0	0

Table 4-1

Application:

Construct a circuit of $\bar{A} \bar{C} + \bar{B} \bar{C}$ and show that this function is logically equivalent of $(\bar{A} + \bar{B}) \bar{C}$.

STEP 5

APPLICATION OF BOOLEAN ALGEBRA

Purpose:

1. To simplify a complex function by Boolean algebra.

Required Components and Equipments:

1. RIMS Training System
2. 7400×1, 7402×1

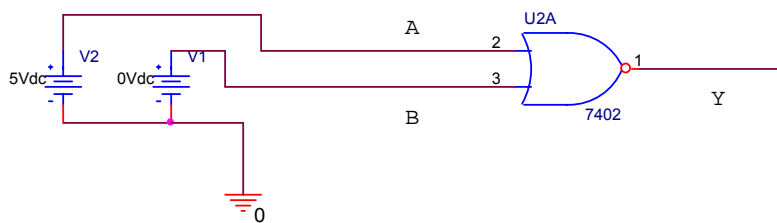
Diagram of Circuit:

Fig. 5-1

Procedure:

Step 1: Construct the circuit show in Fig. 5-1 (a) on the breadboard. Remember connecting pin 7 to ground and pin 14 to +5V as in fig. 5-2.

Step 2: Connect input points A and B to any of the Data switches and point Y to the logic probe.

Step 3: Switch on the system and using all possible binary inputs tabulate the result as shown in table 5-1.

Result:

A	B	Y
0	0	0
0	1	1
1	0	0
1	1	1

Table 5-1

The function of this circuit is identical to Exclusive OR (\overline{XOR}). So we can simplify the Boolean equation

$Y = [(A) (AB)] [(B) (AB)]$ into $Y = AB + A\bar{B}$. The students should be applying to verify this result. Now implement the simplified Boolean expression $Y = \bar{A}B + A\bar{B}$ using AND, OR and NOT gates and verify that the output is same as in table 5-1 for various binary inputs.

Application:

Construct the following circuit on your DEV-2765 verify the function is equal to XOR.

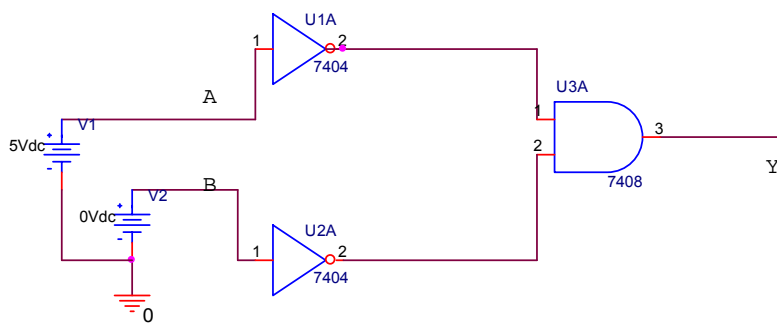


Fig 5-2

STEP 6

DIODE RESISTOR LOGIC – AND

Purpose:

1. From this experiment, study a special type of diode network, the logic circuit.
2. To examine the operation of diode resistor logic AND, and determine its Logical properties.
3. Derive the truth table of AND gate, and verify of its logic equation.

Required Components and Equipments:

1. 1N4148 silicon diode ×3
2. 1KΩ resistor ×1
3. RIMS Training System

Diagram of Circuit:

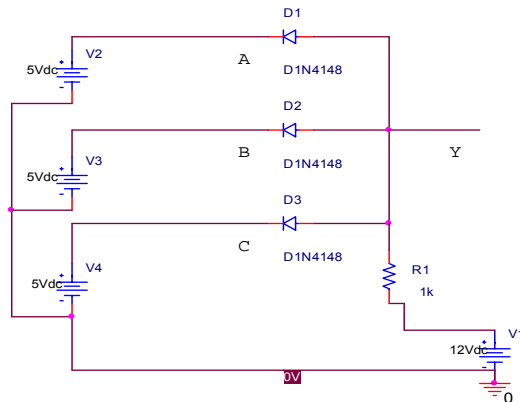


Fig 6-1

Procedure:

Step 1: Install the components of Fig. 6-1 on the breadboard and link the connection correctly.

Step 2: Connect the “+V” point of DC Power Supply to “+” point of DVM, “GND” point of DC Power Supply to “-“point of DVM.

Step 3: Link point A, B, C of Fig. 6-1 to Data Switches “0”, “1”, “2” respectively Connect point Y of Fig.6-1 to 8 Bit LED Display “0”.

Step 4: Change state of Data Switches “0”, “1”, and “2” between “0” or “1” position observe the situation of LED Display “0”. When it is lighting, indicates Logic “1” otherwise indicate logic “0”.

Step 5: Fill in the truth table of Fig. 6-2 according to you obtained from your experiment.

A	B	C	Y
0	0	0	
0	0	1	
0	1	0	
0	1	1	
1	0	0	
1	0	1	
1	1	0	
1	1	1	

Fig 6-2

Result:

After finished this experiment the result will like as follows:

A	B	C	Y
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	0
1	0	0	0
1	0	1	0
1	1	0	0
1	1	1	1

Compare your result with above, to determine if you made anything wrong. If there is any errors, rechecked the components and circuit layout connection and repeat the measurements.

Application:

You already have the experience for uniting AND gate by using only diodes and resistors. Use the same components and equipments as above to design an OR Gate, and verify its truth table.

STEP 7**EXCLUSIVE OR USING BASIC LOGIC GATE****Purpose:**

To combine basic logic gates to form an XOR gate and verify its truth table.

Required Components and Equipments:

1. RIMS Training System
2. 7404 ×1, 7408 ×1, 7432 ×1, 7400 × 2

Diagram of Circuit:

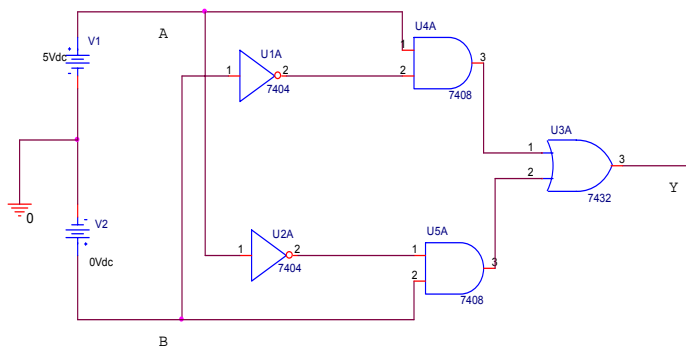


Fig 7-1

Procedure:

Step 1: Construct the circuit show in Fig. 7-1 on the breadboard

Step 2: Connect input point A and B to any of the Data switches and point Y to the logic probe

Step 3: Switch on the system and using all possible binary inputs tabulate the result as shown in table 7-1.

Result:

A	B	Y
0	0	0
0	1	1
1	0	1
1	1	0

Table 7-1

Application:

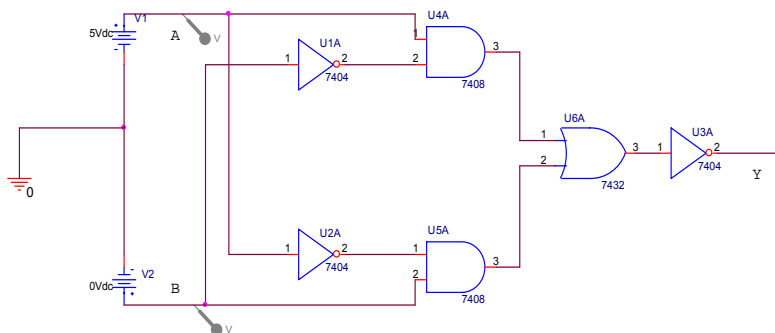
Construct circuit for following logic gates Exclusive NOR using the logic gates.

STEP 8**EXCLUSIVE NOR USING BASIC LOGIC GATE****Purpose:**

1. For understanding the logic function of Exclusive NOR.
2. This experiment is to demonstrate the input and output relationships of XNOR gate by constructing their associated truth table.
3. From this experiment you can exercise how to design the XNOR using the basic logic gate.

Required Components and Equipments:

1. RIMS Training System
1. 7404 ×1, 7408 ×1, 7432 ×1, 7400 × 2

Diagram of Circuit:**Fig 8-1****Procedure:**

Step 1: Plug required IC's into the breadboard of DEV-2765, and supply the correct power to these IC's (pin 14 connect to +5v and pin 7 to GND). Performed the connection according to Fig. 8-1

Step 2: Connect input "A" point to Data Switch "0", input "B" point to Data Switch "1", then connect output "Y" point to the "IN" of 3 State Logic Probe and the "GND" of 3 State Logic Probe must be connected properly.

Step 3: Change both of the Data Switch "0" and "1" position, then observe the display of 3 State Logic Probe.

Step 4: After you have observed the result of display $\overline{A \oplus B}$, fill out the truth table in Fig. 8-1 to Verify the Boolean algebra of XNOR $Y = A \oplus B + AB$.

A	B	Y
0	0	
0	1	
1	0	
1	1	

Table 8-2

Result:

A	B	Y
0	0	0
0	1	1
1	0	1
1	1	0

Application:

Design a circuit using only NAND gates to function as the XNOR gate and perform the experiment.

STEP 9

DEMULTIPLEXER – USING THE 74138 IC

Purpose:

1. To establish the concept of de multiplexer.
2. To give you experience working with multiplexing in general.
3. To verify the basic operation principles of a 74s138 de multiplexer IC.

Required Components and Equipments:

1. IC 74138
2. RIMS Training System

Diagram of Circuit:

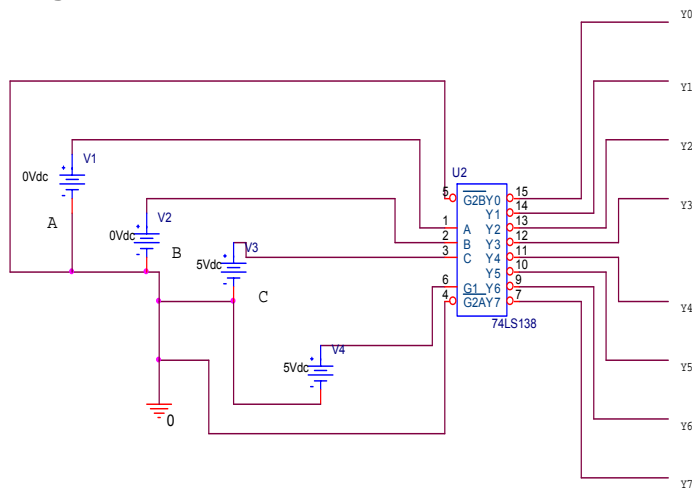


Fig 9-1

Procedure:

Step 1: Construct the circuit of Fig. 9-1 on the breadboard.

Connect 74138's pin 16 to +5v, and its pin 8 to ground.

Step 2: Connect point C, B, A of Fig, 9-1 to Data Switches "0"

Step 3: First, set the three Date Switches to "0"position, and observe the seven LED's Condition. If LED lights, it indicates there has no output, otherwise if LED is dark. It indicates there has an output. Record the output pin to Fig.9-2.

Step 4: Continuously, change the state of the three Data Switches as shown in Fig. 9-2, and write down the output result to the output column of Fig, 9-2.

A	B	C	Output
0	0	0	
0	0	1	
0	1	0	
0	1	1	
1	0	0	
1	0	1	
1	1	0	
1	1	1	

Table: 9-1

Result:

Make certain that G1 is connected to +5v, and G2A and G2B connected to ground. The final results are Fig. 9-3

A	B	C	Output
0	0	0	Y ₀
0	0	1	Y ₁
0	1	0	Y ₂
0	1	1	Y ₃
1	0	0	Y ₄
1	0	1	Y ₅
1	1	0	Y ₆
1	1	1	Y ₇

Application:

If G1 is connected to ground or either G2A or G2B is connected to +5v, it will have no output. Try these!

STEP 10 SYNCHRONOUS UP-COUNTER

Purpose:

T understands the logic function neither of exclusive NOR by constructing the associated truth table.

Required Components and Equipments:

1. Oscilloscope × 1
2. 7404 × 1, 7408 × 1, 7476 × 2
3. 1KΩ resistor × 3
4. RIMS Training System

Diagram of Circuit:

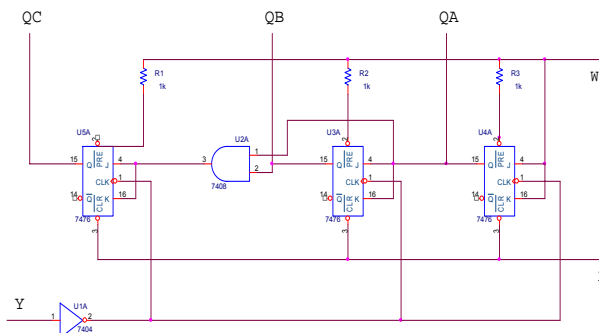


Fig 10-1

Procedure:

Step 1: Construction the circuit of fig, 10-1 onto the breadboard. Remember to connect IC 7476's pin 5 to +5v, pin 13 to ground , and IC 7404 and 7408's pin 14 to +5v , pin 7 to ground.

Step 2: Connect point W Fig. 10-1 to +5V, point X to Digital Inputs 0 and point Y to Data Switches "1". Next connect point Q_C to 8 Bit LED Display's "0" position, point Q_B to "1" position Q_A to "2" position.

Step 3: Cycle Data Switches "0"to "0" then "1" position until all LED's ("0" "1","2") and dark. Leave Data Switches "0" in the "1" position

Step 4: Cycle Data Switches "1"to "1" then "0" position nine times, and simultaneously observe the status of 3 LED's. It is logic 1 when LED is light, and it is logic 0 when LED is dark.

Step 5: Record the state you observe in the truth table of Fig.10-2.

	Present State			Next Sate		
	Q _C	Q _B	Q _A	Q _C	Q _B	Q _A
0	0	0	0			
1						
2						
3						
4						
5						
6						
7						
0						

Fig 10-2**Result:**

If there is not any problem, the result form your experience will be like as Fig. 10-3.

	Present State			Next State		
	Q _C	Q _B	Q _A	Q _C	Q _B	Q _A
0	0	0	0	0	0	1
1	0	0	1	0	1	0
2	0	1	0	0	1	1
3	0	1	1	1	0	0
4	1	0	0	1	0	1

5	1	0	1	1	1	0
6	1	1	0	1	1	1
7	1	1	1	0	0	0
8	0	0	0	0	0	1

Application:

Remove Data Switches "1" from point Y and connect point Y to square wave of function Generator Adjust square waves to proper frequency using your oscilloscope measure the output waveforms of point Q_A, Q_B, and Q_C by oscilloscope. Measure the output waveform of point Q_A, Q_B and Q_C by oscilloscope. Plot the output wave forms down and observe their action

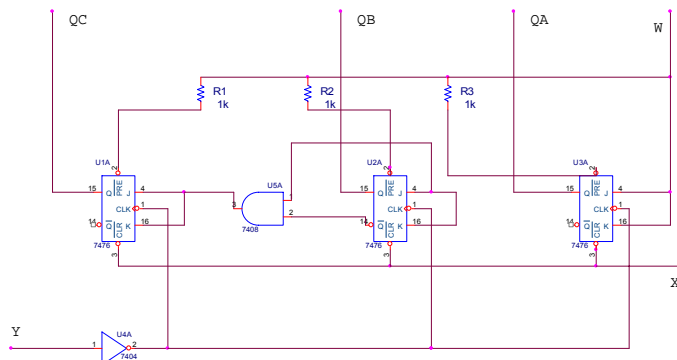
STEP 11	SYNCHRONOUS DOWN- COUNTER
----------------	----------------------------------

Purpose:

For understanding the logic function of exclusive NOR. This experiment is to demonstrate the input and output relationships of XNOR gate by constructing their associated truth table. From this experiment you can exercise how to design the XNOR using basic logic gate.

Required Components and Equipments:

1. Oscilloscope
2. 7404 ×1, 7408 ×1, 7476 ×2
3. 1KΩ resistor × 3.
4. RIMS Trainer DEV-2765

Diagram of Circuit:**Fig 11-1**

Procedure:

Step 1: Install the circuit of Fig. 11-1 on the breadboard. Remember to connect IC 7476's pin 5 to +5v , pin 13 to ground , and 2C 7404 and 7408's pin 14 to +5v pin 7 to ground.

Step 2: Link point W of Fig, 11-1 to +5v of DC Power Supply Point x to Data Switches "0", and point Y to Data Switches "1". Then connect point QC to 12 Bit LED Display's "0" position, and point Q_A to "2" position.

Step 3: Change Data Switches "0" to "0" then "1" position till all of LED's are dark, and leave Data Switches "0" in the "1" position.

Step 4: Exchange Data Switches "1" to "1" then "0" position nine times, and simultaneously observe the situation of the three LED's. LED is light when the output is in logic 1, and LED is dark if the output is in logic 0.

Step 5: Record the situation what you have observe in the truth table of Fig.11-2

	Present State			Next State		
	Q _C	Q _B	Q _A	Q _C	Q _B	Q _C
0	0	0	0			
1						
2						
3						
4						
5						
6						
7						
0						

Table.11-1

Result:

The result will have eight different states of this experiment, so this circuit is also called modulo-8 counter. The truth table we made is as Fig, 11-3.

	Present Status			Next State		
	Q _C	Q _B	Q _A	Q _C	Q _B	Q _A
0	0	0	0	1	1	1
1	1	1	1	1	1	0
2	1	1	0	1	0	1
3	1	0	1	1	0	0
4	1	0	0	0	1	1
5	0	1	1	0	1	0
6	0	1	0	0	0	1
7	0	0	1	0	0	0
0	0	0	0	1	1	1

Table 11-3**Application:**

Use oscilloscope to adjust the square wave of Function Generator to have proper output waveform. Remove Data Switches "1" from point Y and connect point Y to the square wave. Next, use oscilloscope to measure the output waveform of point Q_C, Q_B and Q_A.

Draw the output waveform you have seen at the oscilloscope and observe their behaviors.

STEP 12	THE SCHMITT TRIGGER
----------------	----------------------------

Purpose:

This experiment is just only to adjust the upper trip point, lower trip point, and hysteresis of a digital. Schmitt trigger circuit. After finishing this experiment,

You will learn the concept of how Schmitt trigger is working.

Required Components and Equipments:

1. 7403 × 1
2. IN4149 diode × 1
3. 27KΩ resistor × 1, 812KΩ resistor × 1, 516KΩ resistor × 3, 2.7KΩ resistor × 1, 1KΩ resistor × 3, 820KΩ resistor × 1, 680KΩ resistor × 1, 620 KΩ resistor × 1, 560 KΩ resistor × 11

KΩ resistor ×1.

Diagram of Circuit:

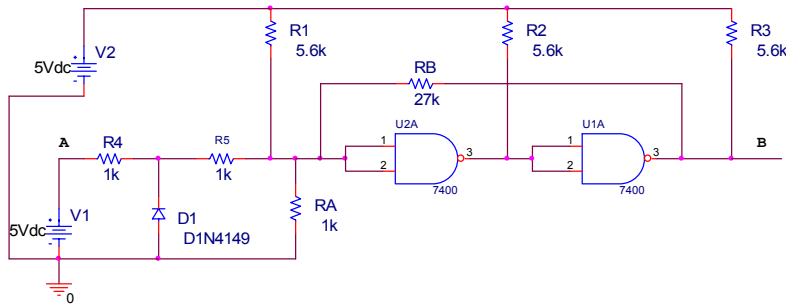


Fig.12-1

Procedure:

Step 1: Construct the circuit of Fig, 12-1 on the breadboard. Remember, IC7403’s pin 14 connects to +5v, and its pin 7 connect to ground.

Step 2: First, RA has a value of 1 KΩ resistor, and RB to be fixed at 27 KΩ, connect output of point B to 12-Bit LED Display “0” position.

Step 3: Set DVM to +5v range, and connect it between point A and ground. Adjust the KΩ pot S0 the DVM reads 0V.

Step 4: Turn the KΩ pot carefully until the LED “0” light. Once the LED “0” is lighting, stop turning the 1KΩ pot. Record the readout value of DVM which has been connected between point A and ground into the UTP column of fig. 12-2. That value is the upper trip point.

RA	UTP	LPT	Hysteresis
1KΩ			
820KΩ			
680KΩ			
620KΩ			
560KΩ			

Table 12-1

Step 5: Adjust the 1KΩ pot to increase the input voltage, to make sure the circuit is past the UPT and in the voltage region where the LED “0” will remain on.

Step 6: Next, slowly turn back the 1KΩ pot until the LED “0” goes off. Record the value you observed on DVM into the LPT column of Fig, 12-2. This value is the lower trip point.

Step 7: Exchange the different value of R_A listed in Fig 12-2, and repeat step 4 to step 6 for each value of R_A .

Step 8: As the LTP and LTP column completed, compute the hysteretic values by UPT-LTP. Record these values in the hysteretic column of Fig.12-2.

Result:

When the resistance of R_A decreases, the voltage for the UPT and LTP increase. Your results of this experiment may differ from ours. Ours result like as Fig, 12-3.

RA	UTP	LTP	Hysteresis
1 K Ω	1.4v	1.1v	0.3v
820K Ω	1.7v	1.3v	0.4v
680K Ω	2.2v	2.0v	0.2v
620K Ω	2.7v	2.5v	0.2v
560K Ω	3.3v	3.0v	0.3v

Table 12-2

Application:

Exchange R_A to be fixed at 680K Ω and R_B will be varied. The R_B will be 2.7 K Ω , 812K Ω and 27 K Ω , then repeat the step 4 to step 6 and record the result. Observe the varying situation of UTP, LPT, and Hysteresis

STEP 13	OSCILLATOR-USING CMOS
----------------	------------------------------

Purpose:

1. To practice how to create square waveform by using CMOS inverters.
2. To study the method of finding the frequency of the oscillator.

Required Components and Equipments:

1. 74C04 \times 1
2. 10K Ω resistor \times 1, 10K Ω resistor \times 1.
3. 100 μ F/ capacitor \times 1.
4. RIMS Training System

Diagram of Circuit:

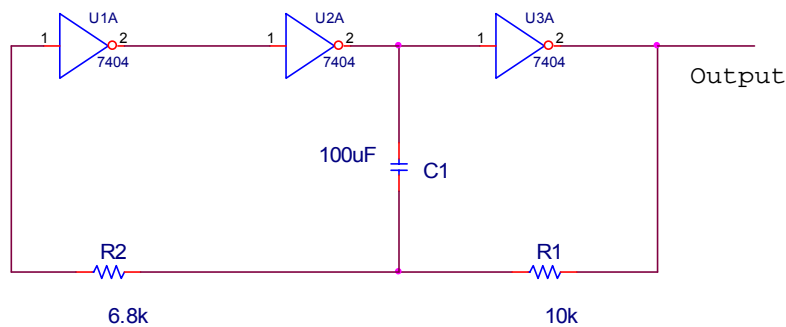


Fig.13-1

Procedure:

Step 1: This oscillator is good low-frequency stability. The duty cycle approaches 50%. This configuration of circuit has vibrated frequency such as

$$f = \frac{1}{2C (0.405R_{eq} + 0.693 R_1)}$$

Where

$$R_{eq} = \frac{R_1 R_2}{R_1 + R_2}$$

Step 2: Install the circuit of Fig 13-1 on the breadboard. Remember; connect 74C04's Pin 14 to +5v, and its pin 7 to ground. It's true that a 35v capacitor can withstand reverse polarities of less than 5v. Connect output point Y to 8 Bit LED Display "0".

Step 3: When the circuit is oscillating, this is one pulse when LED "0" light then darkens. Count the number of pulse, p that occur in 10 seconds and calculate the frequency

$$f = \frac{P}{10} \text{ Hz.}$$

Step 4: According to the formula of finding frequency, calculate the frequency and compare the result with that of step 3 above $f = \text{Hz}$

Result:

Your experiment frequency should be fairly close to the calculated frequency. The difference between the two frequencies may be due to the differences in component tolerances. The experiment frequency is 0.5Hz that there are pulses in 10 seconds, and the calculated frequency can be

obtained as follows:

$$R_{eq} = \frac{R_1 R_2}{R_1 + R_2} = \frac{10 \times 6.8}{10 + 6.8} = 4047.6 \Omega$$

$$f = \frac{1}{2C (0.405 R_{eq} + 0.693 R_1)}$$

$$= \frac{1}{2(100 \times 10^{-6}) ((0.405 \times 4047.6) + (0.693 \times 10^4))}$$

$$\frac{5 \times 10^3}{8569.28} = 0.58 \text{ Hz.}$$

Application:

The different resistance between R_1 and R_2 will generate distinct frequency value. Try to make $R_1 = R_2$, or $R_1 < R_2$, and calculate the frequency value.

**RIMS****EDUCATION****EU, USA and Canada**

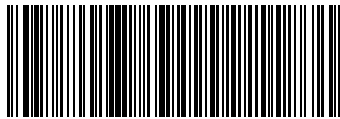
Weston Villa, 37 Wolsey Road, Esher, Surrey
United Kingdom KT10 8NT

www.rims-tech.co.uk

Middle East & Asia Pacific

632-B Chakala Scheme-III Rawalpindi
Pakistan 46000

www.rimsedu.com



DEV2765-00-321

Product Title: RIMS Digital Electronics Trainer

Document Code: DEV2765-00-301

Revision 2.0.1 dated January 2007

© RIMS 1999-2007. All Rights Reserved. No part of this manual is to be copied, modified or sold in any form without prior permission of RIMS EDUCATION

For any further queries please visit our website at

<http://www.rims-tech.co.uk>