RIMS
Research Instrumentation
& Measurement Systems

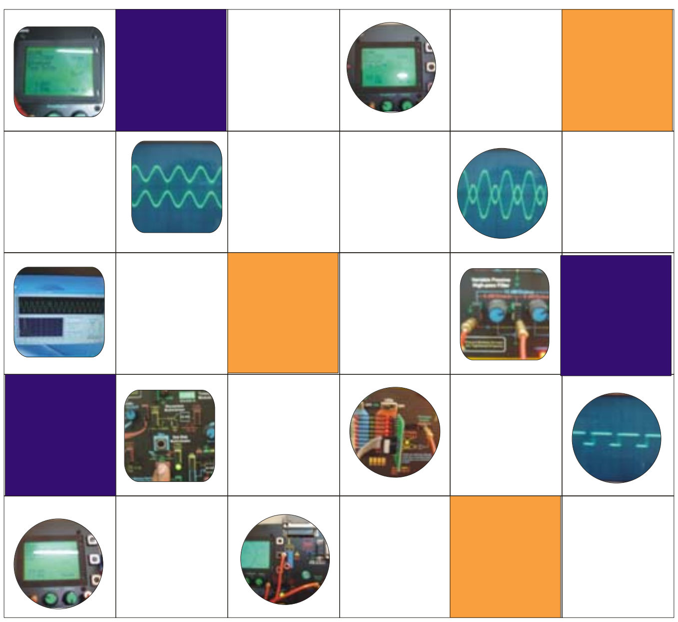
DEV-2766

Advanced Digital Trainer

EXPERIMENTS

Volume 2

PART NO. 2766-00-321



COMPREHENSIVE AND ILLUSTRATED
EASY EXPERIMENTS STARTUP
LAB MANUAL

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Once you have made it through this guide, you will have a firm grip on your lab experiments and operations of the RIMS product you are using. How to get your training equipment operational, basic maintenance and setting up desired experiments will just be a breeze. Everything you need for a quick and easy start is presented here—useful hints and tips makes it simple to conduct your lab and hands-on training sessions. We are happy that you have joined our vast community of over 30 thousand valued users, which grow as we bring you the latest technology at most competitive prices. We value your business and hope that you will enjoy being an important member of the RIMS Education Community.

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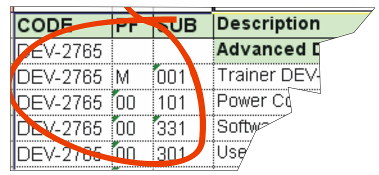
General Information

- ☑ Understanding RIMS part numbers
- ☑ Signals Terminology

1 UNDERSTANDING RIMS PART NUMBERS?

Normally the trainer packaging contains the part numbers that you have ordered. You must understand the order number system for checking your packing note or even for later re-ordering of the equipment.

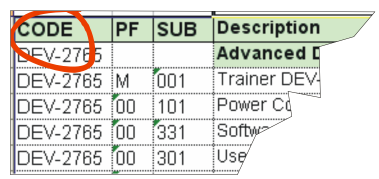


Trainer	-	Prefix	-	Sub-Category
DEV-2766	-	00	-	101

Trainer name is the broad category e.g., 2766 is a Advanced Digital Trainer

The trainer has a prefix that represents the model Number of trainer e.g., ‘M’ or ‘N’

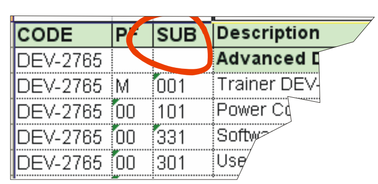
Sub assembly is the hardware component that can be connected to the trainer some modules are compatible with other trainers as well but the part number would only be related to the trainer for which the have been designed



Category is most important feature of this numbering. The under lying structure for category is same for all rims products, the category list is given here,

001-100	Hardware ID
101-200	Cables & Accessories
201-300	Special Attachments
301-400	Data Pack and Media
401-500	Services, Freight and Installations
501-600	Extended Warranties

Here are some common sub categories



101-110	Power Cord
111-120	Interconnecting aids & Data buses
121-130	Dust Covers
131-140	Bread boarding accessories

141-150	Specialized Power Cables
151-160	Extensions and boards
161-170	Cables Serial and Parallel
171-180	Specialized Cables
301-310	Operation Manuals and User Guide
321-330	Experiment Manuals
331-350	SOFTWARE
401-410	Services, Freight and Installations
501-510	Extended Warranties

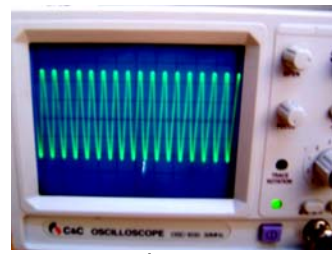
Please use the appropriate order code for either re-ordering components or the equipment from RIMS. The list is subject to further change without altering the existing structure. Please visit RIMS website for any further details about the updates on support pages.

2 Signals Terminology

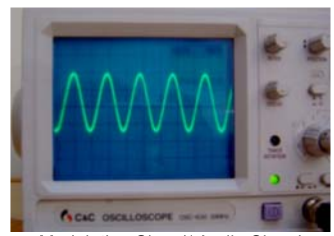
Following terms are used for various signals

Frequency
Number of cycles per second

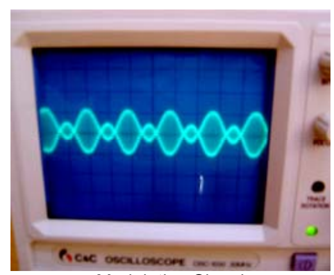
Carrier Signal
Signal that is used as base for carrying signals over long distance usually high frequency signal


Carrier

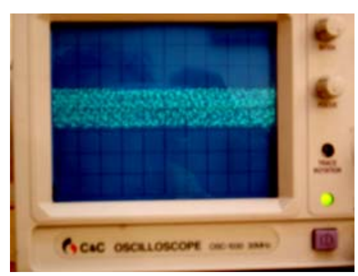
Modulating Signal
Signal that is being modulated such as audio or low frequency signal relative to carrier

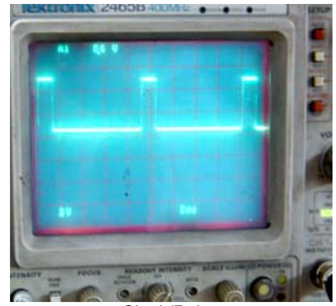

Modulating Signal/ Audio Signal

Modulated Signal
Signal after modulating on the carrier


Modulating Signal

Noise
Uncertainty or randomness in a signal that is represented by sufficient statistics such as mean, variance etc.


Noise

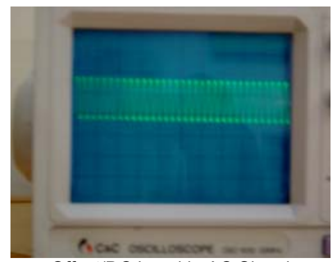

Clock/Pulse

Clock
TTL or square wave for digital control

Voltage
A certain level of signal fixed and not varying e.g., 2.3Volts

Drift
Slowly varying noise (undesired signal)

Offset/Bias
DC level in a signal


Offset/DC Level in AC Signal

Keying
Shifting frequencies within discrete levels

Audio Signal
Normally 300-3500Hz for communications application. Audible range is 20-20KHz, but the telephonic bandwidth is one given above. Above 10KHz and below 300Hz is considered as HI-FI (high fidelity)

Sampling Frequency
Rate at which a signal is digitized by a analog to digital converter

Power
Signal for driving the devices and running the system electronic, while other electronics signals are referred to as signal

Welcome to RIMS Advanced Digital Trainer

List of experiments:

1. Digital Logic Trainer Familiarization (from User manual)
2. AND, OR, NOT Gate
3. XOR
4. De Morgan's Law (I)
5. De Morgan's Law (II)
6. Implementing Boolean Functions
7. Half And Full Adder Designing

Product Title: EXPERIMENTS
Document Code: DEV2766-00-321
Revision 2.0.0 dated February 2007

STEP 1	DIGITAL LOGIC TRAINER FAMILIARIZATION

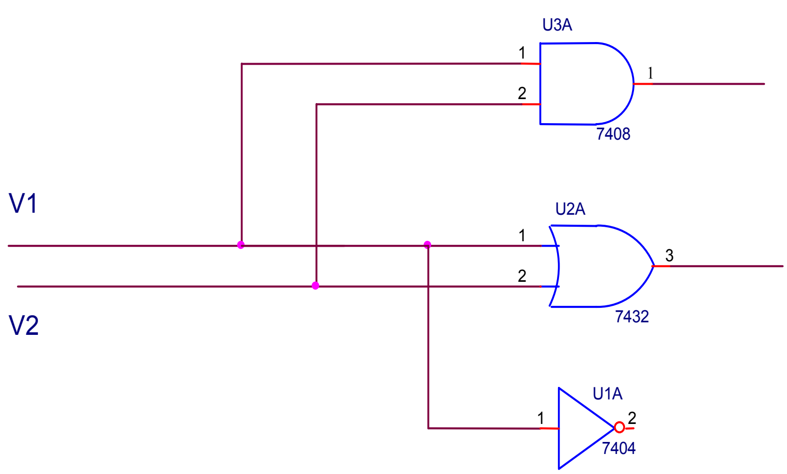
See from user manual

STEP 2	FUNDAMENTAL LOGIC GATES- AND, OR, NOT

Objective:
To show the input and output relationship of 2-input AND, OR, and 1-input NOT gates by constructing their truth tables.

Required Components and Equipments:
7404×1, 7408×1, 7432×1

Diagram of Circuit:



Procedure:
Step 1: Construct the circuit of the figure above on the breadboard. Remember each IC's pin 14 is connected to "+5V" DC Power Supply and pin 7 to "GND" taken from your trainer.

Step 2: Connect the inputs of the gates to two Digital Inputs switches and the outputs of the three gates to three Digital Outputs on your trainer.

Step 3: Try all possible value of V_1 and V_2 inputs as shown in the table below and observe the outputs through their corresponding LEDs. When the LED is ON this indicates logic 1 and if the LED is OFF, this is logic 0. The inputs and outputs in the form of a truth table are shown in the table below.

V_1	V_2	Y_1	Y_2	Y_3
0	0	0	0	1
0	1	0	1	1
1	0	0	1	0
1	1	1	1	0

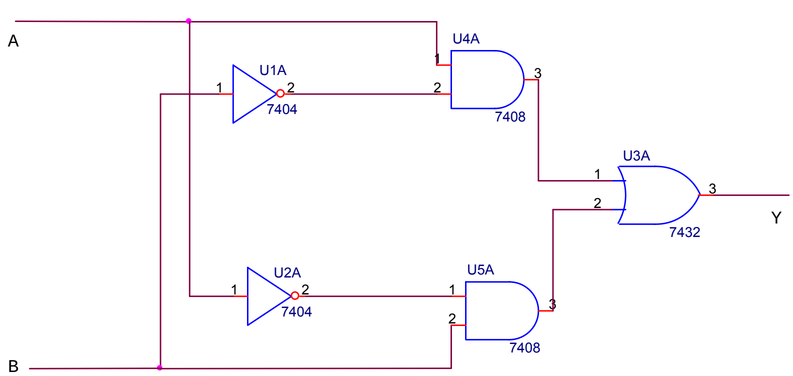
STEP 3	EXCLUSIVE OR USING BASIC LOGIC GATE

Objective:
To combine basic logic gates to form an XOR gate and verify its truth table.

Theory:
An XOR gate output relationship is determined by the expression ÁB + AB́. In this experiment, we implement XOR gate using simpler gates.

Required Components and Equipments:
1. 7404 ×1, 7408 ×1, 7432 ×1, 7400 × 2

Diagram of Circuit:



A	B	Y
0	0	0
0	1	1
1	0	1
1	1	0

Procedure:

Step 1: Construct the circuit shown in the figure on the breadboard.

Step 2: Connect the inputs of the gates to two Digital Inputs switches and connect output of the gate to a Digital Output on your trainer.

Step 3: Try all possible value of A and B inputs as shown in the above table and observe the output through the corresponding LED. Observe that the output is the same as that for an XOR gate.

STEP 4	DE MORGAN'S LAW (I)

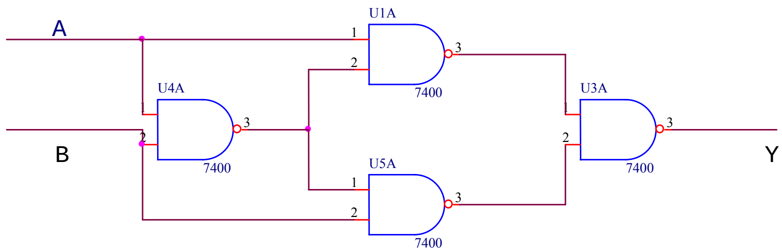
Objective:
To verify the De Morgan's Law (AB)́ = Á+B.́

Theory
One of De Morgan's Laws is (AB)́=Á+B́. This means that the NAND gate function is equivalent to OR gate function with complemented inputs. From this experiment you can understand how to exchange gates for other gates.

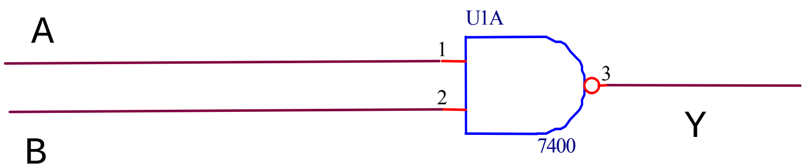
Required Components and Equipments:

1. 7400×1, 7408×1, 7432×1

Diagram of Circuit:



(A)



(B)

A	B	Y=(A+B)´	Y=A´ B´
0	0	1	1
0	1	0	0
1	0	0	0
1	1	0	0

Procedure:

Step 1: Construct separately the circuits shown in the above figures.

Step 2: Connect the inputs of the gates to two Digital Inputs switches and connect output of the gates to two Digital Outputs on your trainer.

Step 3: Try all possible value of A and B inputs as shown in table and observe the outputs through their corresponding LEDs. When the LED is ON this indicates logic 1 and if the LED is OFF, this is logic 0. The inputs and outputs in the form of a truth table as shown in the table. Observe that the outputs of both the gates are same in all cases.

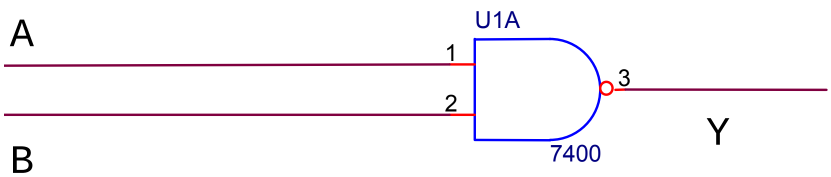
STEP 5	DE MORGAN’S LAW (II)

Objective:
To verify the De Morgan’s Law is that (A+B)´= Á B.́

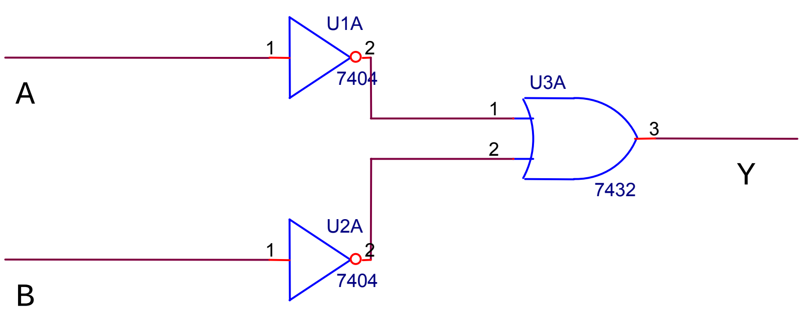
Theory:
One of De Morgan's Law is (A+B)´ = ÁB́. This means that the NOR gate function is equivalent to AND gate function with complemented inputs.

Required Components and Equipments:
7400×1, 7432×1

Diagram of Circuit:



(A)



(B)

A	B	Y=AB	Y=A+B
0	0	1	1
0	1	~~1~~	~~1~~
1	0	1	1
1	1	0	0

Procedure:

Step 1: Construct separately the circuits shown in the above figures.

Step 2: Connect the inputs of the gates to two Digital Inputs switches and connect output of the gates to two Digital Outputs on your trainer.

Step 3: Try all possible value of A and B inputs as shown in the table below and observe the outputs through their corresponding LEDs. When the LED is ON this indicates logic 1 and if the LED is OFF, this is logic 0. The inputs and outputs in the form of a truth table are shown in the table above. Observe that the outputs of both the gates are same in all cases.

STEP 6	IMPLEMENTING BOOLEAN FUNCTION

Objective

The objective of this experiment is to construct a given logic function using CMOS logic design techniques. We will also examine how a CMOS inverter behaves when driving a resistive load and problems that can arise when logic circuits are combined.

Introduction

A given logic function can be implemented in CMOS technology by designing the PMOS pull-up part and the NMOS pull-down part, separately. The PMOS structure is then placed on top of the NMOS structure, with the appropriate power supply and ground connections. The NMOS structure is designed directly from the logical expression by using parallel transistors for OR operation and series transistors for AND operation. The PMOS structure is obtained from the dual of the logical expression, i.e. replacing AND operations by OR operations, and vice versa.

Prelab

Design a CMOS logic circuit that can implement the following function:
F = A'BC + A'BC' + ABC' + ABC + AB'C'
Using positive logic conventions write the truth table for the function and simplify it as much as possible using a K-map. Use a 1's covering and a 0's covering to see if one method results in a simpler design. Draw the schematics for the CMOS logic network.

Assignment

Build and test the CMOS logic circuit designed in prelab. Fill in the values of the truth table on the check-off sheet and answer the questions regarding the CMOS logic circuit design.
Test the effects of resistive loading on the CMOS logic circuit. If your logic circuit does not have an inverter at the output, add one using a CMOS configuration. Then, one at a time, connect each resistor in the table below between the output and ground. Measure the effects on both the PMOS and NMOS stages of the logic circuit. Make sure you have an input combination, which will produce logic ‘1’ at the output (i.e. A = 1, B = 1, C = 1). Measure the corresponding output voltages. Then, one at a time, connect each resistor between the output node and VDD. Give inputs, which result in a logic ‘0’ output (i.e. A = 1, B = 0, C = 1) and measure the resulting output voltages. Record these values in the table on the check-off sheet.

Report

What effect did the resistive loading have on the logic network for both cases? Was there any difference in the effects of resistors pulled high or low? If so, what might be the cause?

STEP 7	HALF AND FULL ADDER DESIGNING

Objective

To provide hands-on experience with basic gates design to build and test different variations of a half and full adder circuit.

Suggested equipment list:

Qty	Description
1	7432,7408,7486
1	5V power supply
1	Oscilloscope with probe
1	Voltmeter
8	2.5K resistor 1/4W
8	LED
2	10k resistor 1/4W
1	Signal generator

As needed various TTL logic gates can be used to implement designs

Procedure:

1. Design a 2 bit half adder and full adder. The half adder implements 2bit a two bit adder without a carry input. The full adder implements a 2 bit adder with a 3 carry input. Use a voltmeter to confirm that the power supply voltage is 5 volts. Add LED's and current-limiting resistors to the 3 outputs to make them observable. Using function generator to generate toggle input. Or in the input to get a one connects that input to a Vcc and to get a zero connect it to ground. Using the LEDs you can verify that the outputs are correct.

2. Test the system to make sure the adder and the

output display all function correctly.

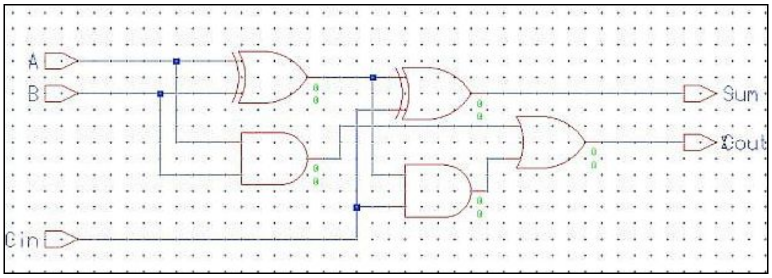


Figure 1: Screen Shot of design in Mentor graphic
Half Adder

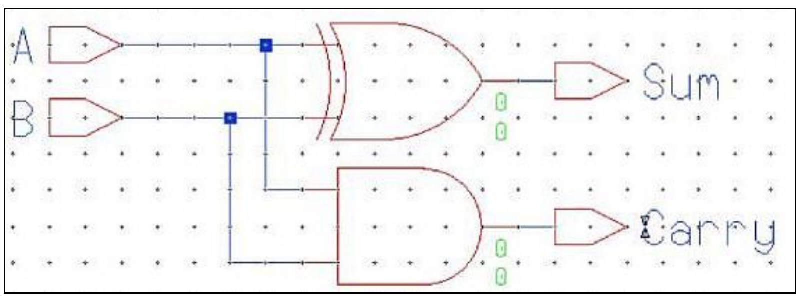


Figure 2: Screen Shot of design in Mentor graphic
Full Adder

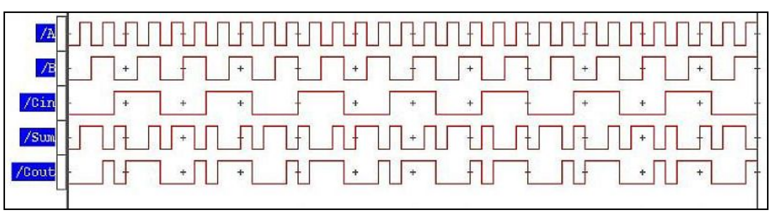


Figure 3: Screen Shot of trace in Mentor graphics
Half Adder

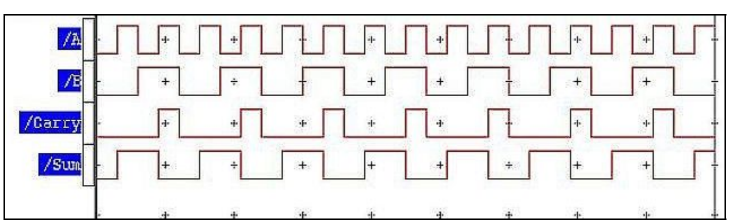


Figure 4: Screen Shot of trace in Mentor graphics
Full Adder

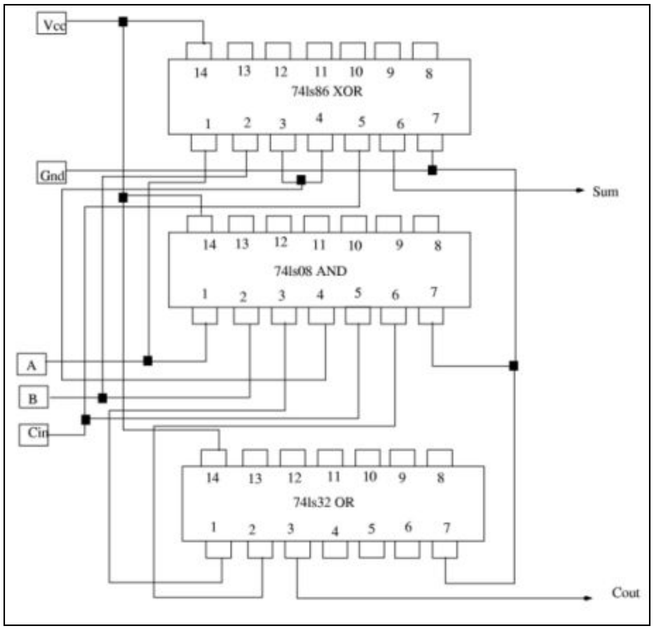


Figure : Circuit Diagram Full Adder (Not complete)

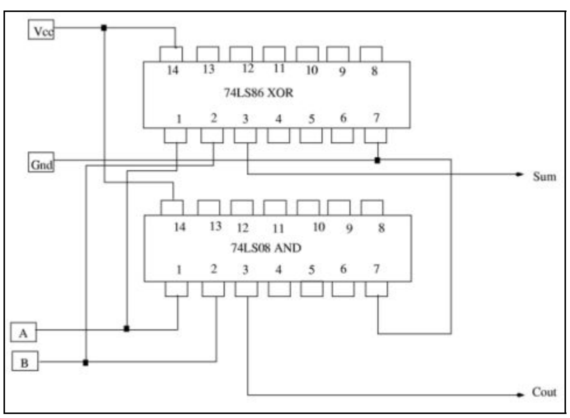


Figure : Circuit Diagram Half Adder

Pre-Lab – Understanding Adders

1. Create the truth table for 3 bit full adder?

2. Draw the gate level implementation of 3 bit Full adder circuits?

3. How to implement Half and Full adders using only NAND gates?

4. How to implement Half and Full adders using only NOR gates?

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Product Title: RIMS Advanced Digital Trainer
Document Code: DEV2766-00-321
Revision 2.0.1 dated February 2007

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