RIMS
Research Instrumentation
& Measurement Systems

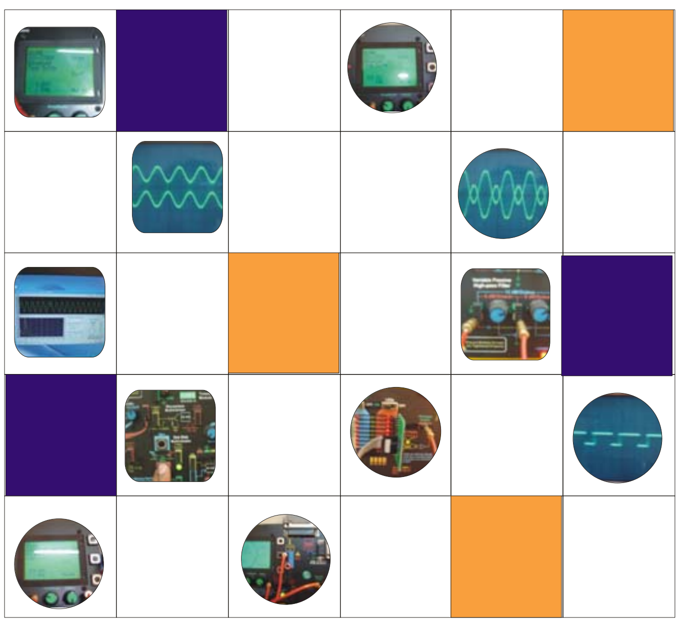
DEV-2769

Advanced Electronics Trainer

EXPERIMENTS

Volume 3

PART NO. 2769-00-321



COMPREHENSIVE AND ILLUSTRATED
EASY EXPERIMENTS STARTUP
LAB MANUAL

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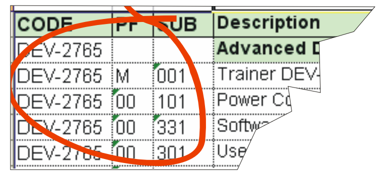
General Information

- ☑ Understanding RIMS part numbers
- ☑ Signals Terminology

1	UNDERSTANDING RIMS PART NUMBERS?

Normally the trainer packaging contains the part numbers that you have ordered. You must understand the order number system for checking your packing note or even for later re-ordering of the equipment.

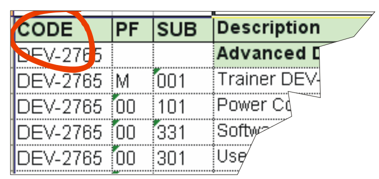


Trainer	-	Prefix	-	Sub-Category
DEV-2769	-	00	-	101

Trainer name is the broad category e.g., 2769 is a Advanced Electronics Trainer

The trainer has a prefix that represents the model Number of trainer e.g., ‘M’ or ‘N’

Sub assembly is the hardware component that can be connected to the trainer some modules are compatible with other trainers as well but the part number would only be related to the trainer for which the have been designed



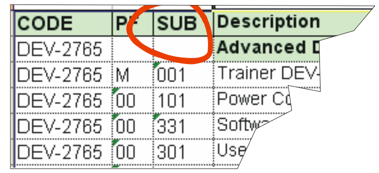
Category is most important feature of this numbering. The under lying structure for category is same for all rims products, the category list is given here,

001-100	Hardware ID
101-200	Cables & Accessories
201-300	Special Attachments
301-400	Data Pack and Media
401-500	Services, Freight and Installations
501-600	Extended Warranties

Here are some common sub categories

101-110	Power Cord
111-120	Interconnecting aids & Data buses

121-130	Dust Covers
131-140	Bread boarding accessories
141-150	Specialized Power Cables
151-160	Extensions and boards
161-170	Cables Serial and Parallel
171-180	Specialized Cables
301-310	Operation Manuals and User Guide
321-330	Experiment Manuals
331-350	SOFTWARE
401-410	Services, Freight and Installations
501-510	Extended Warranties



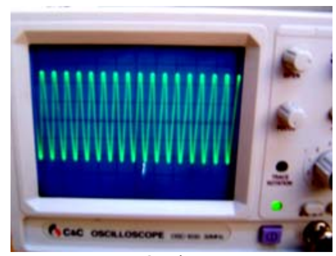
Please use the appropriate order code for either re-ordering components or the equipment from RIMS. The list is subject to further change without altering the existing structure. Please visit RIMS website for any further details about the updates on support pages.

2 SIGNALS TERMINOLOGY

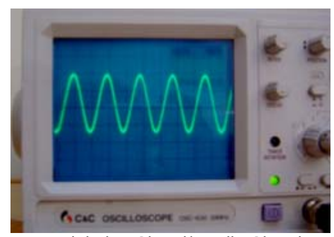
Following terms are used for various signals

Frequency
Number of cycles per second

Carrier Signal
Signal that is used as base for carrying signals over long distance usually high frequency signal


Carrier

Modulating Signal
Signal that is being modulated such as audio or low frequency signal relative to carrier

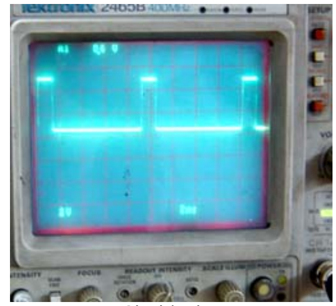

Modulating Signal/ Audio Signal

Modulated Signal
Signal after modulating on the carrier

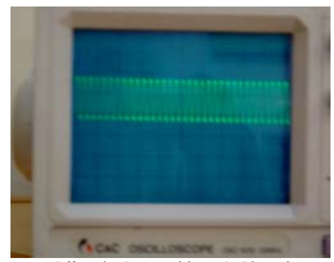

Modulating Signal

Noise
Uncertainty or randomness in a signal that is represented by sufficient statistics such as mean, variance etc.


Noise


Clock/Pulse

Clock
TTL or square wave for digital control


Offset/DC Level in AC Signal

Voltage
A certain level of signal fixed and not varying e.g., 2.3Volts

Drift
Slowly varying noise (undesired signal)

Offset/Bias
DC level in a signal

Keying
Shifting frequencies within discrete levels

Audio Signal
Normally 300-3500Hz for communications application. Audible range is 20-20KHz, but the telephonic bandwidth is one given above. Above 10KHz and below 300Hz is considered as HI-FI (high fidelity)

Sampling Frequency
Rate at which a signal is digitized by a analog to digital converter

Power
Signal for driving the devices and running the system electronic, while other electronics signals are referred to as signal

Welcome to RIMS Advanced Electronics Trainer

List of experiments:

1. Magnitude Comparator Circuits
2. Implementing Encoder & Decoder
3. Implementing Multiplexer
4. Implementing J-K, R-S, D Toggle Flip Flop

Product Title: EXPERIMENTS
Document Code: DEV2769-00-321
Revision 2.0.0 dated February 2007

STEP 1	MAGNITUDE COMPARATOR CIRCUITS

Learning Objectives:

The purpose of this experiment is to introduce magnitude comparators and illustrate some of their applications. The four bit magnitude comparator performs the comparison of straight binary and straight BCD codes providing three outputs indicating the conditions of equal to, greater than, or less than. A magnitude comparator compares the magnitude, i.e. unsigned binary, of two numbers.

Suggested equipment list:

Quantity	Description
1	74LS85
1	5V power supply
1	Voltmeter
1	Oscilloscope with probe
8	2.5K resistor 1/4W
1	Signal generator
8	LED

Theory:

The SN54/74LS85 is a 4-Bit Magnitude Comparator which compares two 4-bit words (A, B), each word having four Parallel Inputs (A0–A3, B0–B3); A3, B3 being the most significant inputs. Operation is not restricted to binary codes; the device will work with any monotonic code. Three Outputs are provided: “A greater than B” ($O_{A>B}$), “A less than B”

($O_{A<B}$), "A equal to B" ($O_{A=B}$). Three Expander Inputs, $I_{A>B}$, $I_{A<B}$, $I_{A=B}$, allow cascading without external gates. For proper compare operation, the Expander Inputs to the least significant position must be connected as follows: $I_{A<B}$= $I_{A>B}$ = L, $I_{A=B}$ = H. For serial (ripple) expansion, the $O_{A>B}$, $O_{A<B}$ and $O_{A=B}$ Outputs are connected respectively to the $I_{A>B}$, $I_{A<B}$, and $I_{A=B}$ Inputs of the next most significant comparator, as shown in Figure 1. Refer to Applications section of data sheet for high speed method of comparing large words.
The Truth Table on the following page describes the operation of the SN54/74LS85 under all possible logic conditions. The upper 11 lines describe the normal operation under all conditions that will occur in a single device or in a series expansion scheme. The lower five lines describe the operation under abnormal conditions on the cascading inputs. These conditions occur when the parallel expansion technique is used.

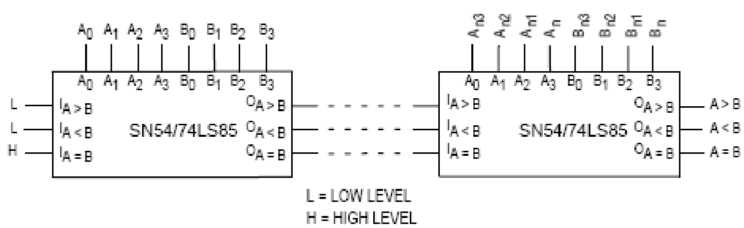
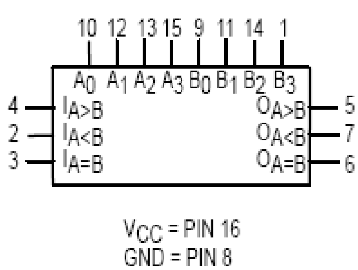


Figure 1. Comparing Two n-Bit Words

Logic Symbol:



Truth Table:

COMPARING INPUTS				CASCADING INPUTS			OUTPUTS		
A_3,B_3	A_2,B_2	A_1,B_1	A_0,B_0	$I_{A>B}$	$I_{A<B}$	$I_{A=B}$	$O_{A>B}$	$O_{A<B}$	$O_{A=B}$
$A_3>B_3$	X	X	X	X	X	X	H	L	L
$A_3<B_3$	X	X	X	X	X	X	L	H	L
$A_3=B_3$	$A_2>B_2$	X	X	X	X	X	H	L	L
$A_3=B_3$	$A_2<B_2$	X	X	X	X	X	L	H	L
$A_3=B_3$	$A_2=B_2$	$A_1>B_1$	X	X	X	X	H	L	L
$A_3=B_3$	$A_2=B_2$	$A_1<B_1$	X	X	X	X	L	H	L
$A_3=B_3$	$A_2=B_2$	$A_1=B1$	$A_0>B_0$	X	X	X	H	L	L
$A_3=B_3$	$A_2=B_2$	$A_1=B_1$	$A_0<B_0$	X	X	X	L	H	L
$A_3=B_3$	$A_2=B_2$	$A_1=B_1$	$A_0=B_0$	H	L	L	H	L	L
$A_3=B_3$	$A_2=B_2$	$A_1=B_1$	$A_0=B_0$	L	H	L	L	H	L
$A_3=B_3$	$A_2=B_2$	$A_1=B_1$	$A_0=B_0$	X	X	H	L	L	H
$A_3=B_3$	$A_2=B_2$	$A_1=B_1$	$A_0=B_0$	H	H	L	L	L	L
$A_3=B_3$	$A_2=B_2$	$A_1=B_1$	$A_0=B_0$	L	L	L	H	H	L

H = HIGH Level
L = LOW Level
X = IMMATERIAL

Procedure:

1. Apply the VCC and ground to the IC 74LS85. Apply the word A equal to 8, by changing word b from 0 to 7 and verify the result.

2. In the same way apply B equal to 8 and change word A from 0 to 7 and verify the result.

3. Now apply to similar word to A and B and verify the result.

STEP 2	ENCODER & DECODER

Purpose

To design & implement the following conversion
1. Binary to Gray code
2. Gray to Binary code
3. BCD to Excess-3
4. Excess-3 to BCD.

Required Components and Equipments

Digital Trainer Kit, IC 7400 (Quad 2 input NAND gate), IC 7404 (Hex inverter) IC 7408 (Quad 2 input AND gate), IC 7432 (Quad 2 input OR gate), IC 7486 (Quad EX-OR gates), Connecting Wires

Theory:

Binary Number System:

The number system with base two is known as the binary number system. Only two symbols are used to represent numbers in this system these are 0 & 1. These are known as bits. It is a positional system that is every position is assigned a specific weight

Codes:

Computer & other digital circuits process data in the binary circuit's process data in the binary format. Various binary codes are used to represent data, which may be num eric, alphabets or special character.

1. Binary Code:

This is used to represent numbers using natural binary form.
Ex. Decimal numbers 23 is to binary 10111.
i.e.(23)10=(10111)2
Binary Coded Decimal (BCD) code:
In this code, decimal digits 0 through 9 are represented by their binary equivalents using four bits & each decimal digit of decimal number is represented by this four-bit code individually.
Ex. Decimal number 23 is equivalent to 001000 11
i.e. (23)10= 0010 0011.
This code is also known as 8-4-2-1 codes. This is a weighted code & arithmetic operation can be performed using this code. It is very convenient & useful code for input & output operations in digital systems.

2. Excess -3 Code:

This is another form of BCD code, in which each decimal digit is coded into a 4 bit binary code. The code for each decimal digit is obtained by adding decimal 3 to the natural BCD code of the digit. It is not a weighted code.
Ex. Decimal 2 is coded as 00 10 + 0011 = 0 10 1 in Execess-3code.

3. Gray Code:

It is very useful code in which a decimal number is represented in binary form in such a way that each Gray-code number differs from the preceding and the succeeding number by a single bit. It is not a weighted code.
Ex. The Gray code for decimal number 5 is 0111 and for 6 it is 0101. These two codes differ by only one bit positional (third from the left)

CODE CONVERSION:
Binary to Gray and Vice Versa.
Let B3 B2 B1 BO be binary code and G3 G2 G1 GO be Gray code.

Truth Table

Decimal	Binary Code				Gray Code			
	B3	B2	B1	B0	G3	G2	G1	G0
0	0	0	0	0	0	0	0	0
1	0	0	0	1	0	0	0	1
2	0	0	1	0	0	0	1	1
3	0	0	1	1	0	0	1	0
4	0	1	0	0	0	1	1	0
5	0	1	0	1	0	1	1	1
6	0	1	1	0	0	1	0	1
7	0	1	1	1	0	1	0	0
8	1	0	0	0	1	0	0	0
9	1	0	0	1	1	0	0	1
10	1	0	1	0	1	0	1	1
11	1	0	1	1	1	0	1	0
12	1	1	0	0	1	1	1	0
13	1	1	0	1	1	1	1	1
14	1	1	1	0	1	1	0	1
15	1	1	1	1	1	1	0	0

The following relations are derived from K-map
A) To convert Binary to Gray

$G3 = B3$

$G2 = B3 \oplus B2$

$G1 = B2 \oplus B1$

$G0 = B1 \oplus B0$

B) To convert Gray to Binary

$B3 = G3$

$B2 = B3 \oplus G2$

$B1 = B2 \oplus G1$
$B0 = B1 \oplus G0$

ii) BCD to Excess-3 and vice versa
Let B3, B2, B1, B0 be a binary code and E3, E2, El, E0 be a Excess-3 code

Truth Table

Decimal	BCD				EXCESS-3			
	B3	B2	B1	B0	E3	E2	E1	E0
0	0	0	0	0	0	0	1	1
1	0	0	0	1	0	1	0	0
2	0	0	1	0	0	1	0	1
3	0	0	1	1	0	1	1	0
4	0	1	0	0	0	1	1	1
5	0	1	0	1	1	0	0	0
6	0	1	1	0	1	0	0	1
7	0	1	1	1	1	0	1	0
8	1	0	0	0	1	0	1	1
9	1	0	0	1	1	1	0	0

Following relations are derived from K-map

A) To convert BCD to Excess-3:

$E3 = B3 + B2\,(BO + B1)$

$E2 = B2\,\overline{B1}\,\overline{BO} + \overline{B2}\,(BO + B1)$
$E\,l = B1$
$E0 = B0$

B) To convert Excess -3 to BCD :

$B3 = E3\,E2 + E3\,El\,E0$

$B2 = \overline{E2}\,\overline{El} + E2\,El\,E0 + E3\,El\,\overline{E0}$
$B1 = El \oplus E0$
$B0 = \overline{E0}$

PROCEDURE:

A) BCD to Gray conversion:

1. Implement the circuit as shown i11 fig. 1 using IC 7486.
2. Give various binary inputs & verify corresponding Gray code outputs.

B) Gray to BCD Conversion:

1. Implements the circuit gives as shown in fig. 2 using IC 7486.
2. Give various Gray code inputs verify corresponding BCD output.

C) BCD to Excess -3 Conversion:

1. Implement the circuit as shown in fig.3 using Ics 7486, 7432 and 7408
2. Give various BCD code inputs and verify corresponding Excess -3 code output.

D) Excess -3 code to BCD conversion:

1. Implement the circuit as shown in fig. 4 using Is 7486,7400, 7432 and 7408.
2. Give various Excess -3 code inputs & verify corresponding BCD outputs.

CONCLUSION:

Different code conversions are studied & implemented using logic gates. Its output is verified.

STEP 3	IMPLEMENTING MULTIPLEXER

Objective:

To understand the functionality of multiplexing.

Suggested equipment list:

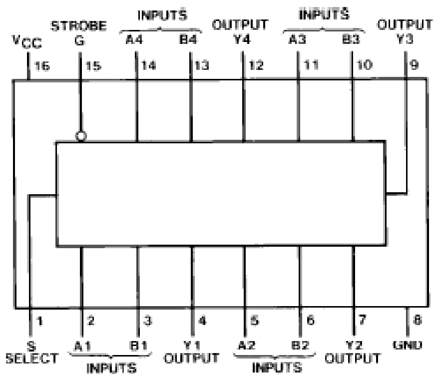
Quantity	Description
1	74LS157, 74LS04, 74LS08, 7425
1	5V power supply
1	Voltmeter
1	Oscilloscope with probe
8	2.5K resistor 1/4W
1	Signal generator
8	LED

Theory:

A multiplexer is a combinatorial circuit that is given a certain number (usually a power of two) data inputs, let us say 2n, and n address inputs used as a binary number to select one of the data inputs. The multiplexer has a single output, which has the same value as the selected data input.

In other words, the multiplexer works like the input selector of a home music system. Only one input is selected at a time, and the selected input is transmitted to the single output. While on the music system, the selection of the input is made manually, the multiplexer chooses its input based on a binary number, the address input.

Logic Symbol:



Truth Table:

Inputs				Output Y	
Strobe	Select	A	B	LS157	LS158
H	X	X	X	L	H
L	L	L	X	L	H
L	L	H	X	H	L
L	H	X	L	L	H
L	H	X	H	H	L

H = High Level, L = Low Level, X = Don't Care

Procedure:

1. Apply the VCC = 5V and ground to the 74LS157. For the first 2-Line to 1-Line multiplexer verify the truth table.

2. Construct a 4-Line to 2-Line multiplexer using the two 2-Line to 1-Line multiplexers.

STEP 4	IMPLEMENTING R-S, J-K, D TOGGLE FLIP FLOP

Objective:

To understand the functionality of different types of Flip Flop.

Suggested equipment list:

Quantity	Description
2	74LS00
1	74LS04
1	5V power supply
1	Voltmeter
1	Oscilloscope with probe
8	2.5K resistor 1/4W
1	Signal generator
8	LED

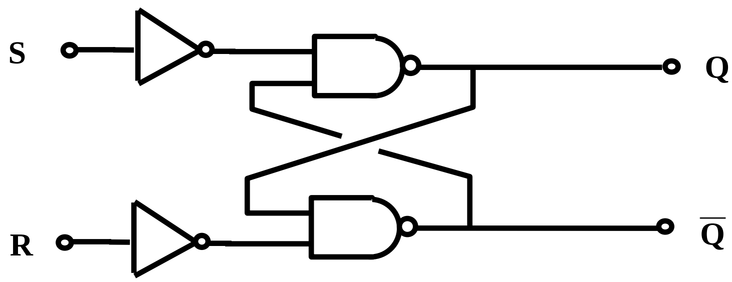
R-S flip flop

Theory:

The elements you have studied so far, gates and inverters, may be used to carry out logic operations, but they exhibit no memory capability; that is, their output states depend only on the instantaneous values of their inputs. Computers require such elements to carry out the processing functions (ordinary arithmetic and Boolean algebraic functions) required in the central processor.
In addition to these devices, however, a computer also requires elements which exhibit “memory” and act like two-state toggle switches, having outputs that can be set to a particular state by some

transient input and remain in that state after the transient disappears. One such element of this kind is the flip-flop; it has an output, either Hi or Lo (1 or 0) which can be switched from one state to the other by applying an appropriate transient input. Flip-flops are used to perform various memory and arithmetic operations in computers.

Logic Circuit:



Truth Table:

R	S	Q	Q'	Comment
0	0	Q	Q'	Hold state
0	1	1	0	Set
1	0	0	1	Reset
1	1	?	?	Avoid

Procedure:

1. Construct the following circuit from a pair of gates in the 74LS00 Quad 2-Input NAND Gate and a pair of inverters.

2. Connect the S (“Set”) and R (“Reset”) inputs to the push-buttons at the bottom (choose the connections that give a voltage that switches to “Hi”

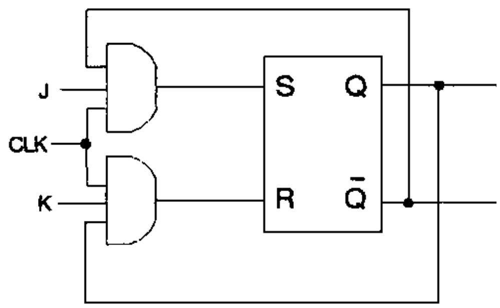
when the button is pressed). Connect the Q and outputs via the BNC connectors to the two (d.c. connected) vertical inputs of a ’scope or DMM.

Note that the state of the outputs is well-defined if either (or both) of the S and R inputs is Hi (5 V). Note also that the system can be in either one of two stable output states when the two inputs (R and S) are both Lo (5V). In which of these two states it finds itself depends on which of S or R was last set to Hi before being returned to Lo.
Verify this characteristic.

J- K flip flop

Theory:
The JK flip-flop augments the behavior of the SR flip-flop by interpreting the S = R = 1 condition as a "flip" command. Specifically, the combination J = 1, K = 0 is a command to set the flip-flop; the combination J = 0, K = 1 is a command to reset the flip-flop; and the combination J = K = 1 is a command to toggle the flip-flop, i.e., change its output to the logical complement of its current value. Setting J = K = 0 results in a D-type flip-flop. The JK flip-flop is therefore a universal flip-flop, because it can be configured to work as an SR flip-flop, a D flip-flop.

Logic Circuit:



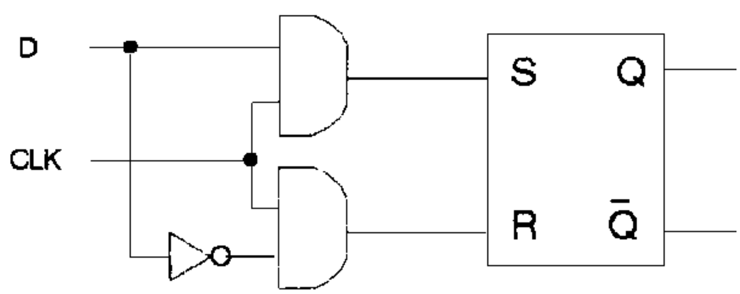
Truth Table:

J	K	Q	Qnext	Comment
0	0	0	0	hold state
0	0	1	1	hold state
0	1	X	0	reset
1	0	X	1	set
1	1	0	1	toggle
1	1	1	0	toggle

D flip flop

Theory:
The D flip-flop can be interpreted as a primitive delay line or zero-order hold, since the data is posted at the output one clock cycle after it arrives at the input. It is called delay flip flop since the output takes the value in the Data-in.

Logic Circuit:



Truth Table:

D	Q
0	0
1	1

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